GP/2818

Attorney Docket No. 15448-0505

#2
04-30-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Alok Jain, et al.

Group Art Unit No.: 2818

Examiner: NYA

Serial No.: 10/029,547

Filed on: December 21, 2001

For: MECHANISM FOR RECOGNIZING AND ABSTRACTING MEMORY STRUCTURES

Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

__X__ 37 C.F.R. §1.97(b).

_____ 37 C.F.R. §1.97(c). If so, then this Information Disclosure Statement includes one of the following:

_____ A statement pursuant to 37 C.F.R. §1.97(e)

_____ 1.97(e)(1) The undersigned hereby states that each item of information contained in this information disclosure statement was first cited in communication from a foreign patent office in a counterpart

foreign application not more than three months prior to the filing of this information disclosure statement.

_____ 1.97(e)(2) The undersigned hereby states that no item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in this information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of this information disclosure statement.

_____ A check for $180.00 for the fee under 37 C.F.R. § 1.17(p).

_____ 37 C.F.R. §1.97(d). If so, then this Information Disclosure Statement includes the following:

_____ A statement pursuant to 37 C.F.R. §1.97(e)

_____. 1.97(e)(1) The undersigned hereby states that each item of information contained in this information disclosure statement was first cited in communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement; OR

_____ 1.97(e)(2) The undersigned hereby states that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of this information disclosure statement.

AND

_____ A check for $180.00 for the fee under 37 C.F.R. §1.17(i) for submission of the Information Disclosure Statement.

_____ 37 C.F.R. §1.97(i). Wherein applicants are submitting references before the grant of a patent to be placed in the file but not considered by the Patent office.

(1) Accordingly, copies of the references as listed on the attached Form PTO 1449 are submitted herewith for placement in the file. No certification or fees are deemed necessary.

Throughout the pendency of this application, please charge any additional fees, including any required extension of time fees, and credit all overpayments to deposit account 50-1302. A duplicate of this sheet is enclosed.

Respectfully submitted,

HICKMAN PALERMO TRUONG & BECKER LLP

Dated: February 27, 2002

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, Washington, D. C. 20231 on February 27, 2002
(Date of Deposit)

Jennifer Newell
(Typed or printed name of person mailing correspondence)

(Signature of person mailing correspondence)

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
15448-0505	10/029,547
APPLICANT: Alok Jain, et al.	
FILING DATE: December 21, 2001	GROUP: 2818

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	"M. Pandey, et al., "Exploiting Symmetry when Verifying Transistor-Level Circuits by Symbolic Trajectory Evaluation," IEEE, Vol. 18, No. 7, July 1999, pp. 918-935.
	D. T. Blaauw, et al., "Functional Abstraction of Logic Gates for Switch-Level Simulation," European Conference on Design Automation, pp. 329-333, February 1991.
	S. Kundu, "GateMaker: A Transistor to Gate Level Model Extractor for Simulation, Automatic Test Pattern Generation and Verification," International Test Conference, pp. 372-381, 1998.
	R. E. Bryant, "Algorithmic Aspects of Symbolic Switch Network Analysis," IEEE Transactions on Computer Aided Design, pp. 618-633, July 1987.
✓	R. E. Bryant, "Boolean Analysis of MOS Circuits," IEEE Transactions on Computer Aided Design, pp. 634-649, July 1987.
	R. E. Bryant, "Extraction of Gate Level Models From Transistor Circuits by Four-Valued Symbolic Analysis," International Conference on Computer Aided Design, pp. 350-353, 1991.
✓	S. Jain, et al., "Automatic Clock Abstraction from Sequential Circuits," Design Automation Conference, pp. 707-711, 1995.
	R. Razdan, et al., "Clock Suppression Techniques for Synchronous Circuits," IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, pp. 1547-1556, October 1993.
	F. Rocheteau, et al., "Tralala: A Fast and Accurate Functional Abstraction Tool For Transistor Netlists," SAME 99, Accessible from http://www.sansistor.com.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.